VARIABLE STEP
POWER FACTOR
PANEL CONTROLLER
VSPFC
v0r2

INSTALLATION
AND
OPERATION
MANUAL

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1. INTRODUCTION

This manual describes the installation and operation of the Variable Step Power Factor Controller VSPFC, version 0 release 2. V0r2 introduces rebooting after a non-recoverable error, factory saved calibration parameters, last error logging and minor code improvements and bug fixes on the previous version (v0r1, March 2013).

The Controller has been designed for power factor control applications with the following features and characteristics:

- Variable compensating capacitance step can be any combination of the driven banks, effectively realizing an up to 4095 step system,
- Twelve bit inputs and outputs to drive up to twelve capacitor bank switches with individual or group fault/error feedback,
- Specific bit output can be assigned to drive a fan as a function of the connected bank sum,
- Operates in compensating or regulating mode,
- Fully programmable parameters and function,
- Single- or three- phase connection,
- Provides all quantities relevant to power factor control applications,
- Complete integration within a Quamatic or similar network or other supervisory systems via an assigned bit input and output pair,
- Simple, self-contained, unattended operation by non-specialist personnel, and
- Standard front panel cut-out dimensions (per DIN 43700).

The Controller provides for different capacitor bank sizes and can be set to function as a power factor regulator or a power factor compensator. At every sampling instant, the Controller calculates the required compensation step and connects/disconnects a combination of banks whose sum is equal or closest to the calculated step value. As an example, four banks sized as x5, x2, x2 and x1 multiples of the smallest required step provide a decade of compensating operation and function as a typical ten equal step system.

In regulator mode the current is detected at the line side and equals to the sum of the load and connected capacitor currents. In this mode the Controller switches capacitor banks in and out of the line to minimize reactive current at the line side. In compensator mode the current is detected at the load side and is equal only to the load current. In this mode the Controller switches the banks in and out of the line to compensate the detected reactive load current as closely as is feasible by the available bank sizes.

The Controller employs a two channel 11 bit analog/digital converter (ADC) to detect the current transformer (CT) apparent current as an absolute magnitude and its phase-detected component (locked to the Controller supply voltage) as a bipolar magnitude. Depending on the mode of control (regulating or compensating) and the type of installation (single- or three- phase), the Controller calculates the load power in KW and the power factor, apparent power in KVA and reactive power in KVAr for the line and the load.

This manual goes through the installation, parameter programming and operation of the Controller and contains additional material in appendices.

2. HARDWARE INSTALLATION

2.1. Hardware Overview

The Controller has the following resources:

- Twelve galvanically isolated bit inputs to interface to the external capacitor bank fault/error feedback or master enable commands,
- Twelve galvanically isolated bit outputs to drive the compensating capacitor bank switches and a fan or fault/error feedback to a master (if enabled),
- Standard 5A current transformer secondary interface,
- Dual standard serial communication port: RS232 for local communications and/or RS485 for connection to Quamatic (and similar) networks and remote sensors,
- Triple isolated output power supply: RS485/RS232 port, internal logic and external interface,
- Five digit plus sign LED display, and
- Four operator switches on the front panel.

The Controller front panel is protected to IP54 and is covered by a polyester membrane. The display digits are visible through a contrast enhancing transparent window and the switches are of the tactile type.

All connections are made at the terminal blocks on the Controller rear. At the rear, but inside, is the power supply protective fuse.

2.2. Mechanical Installation

The Controller is fitted in a standard DIN 43700 138x92 mm opening and is fixed with the supplied holding mechanisms.

2.3. Power Circuit Connection

The Controller is powered with 230 VAC (VSPFC-230 models) or 115 VAC (VSPFC-115 models). The connection is effected at the power terminal block as follows:

Power (115 or 230 VAC) Circuit Connection		
Terminal	**Connection**	**Comments**
L	Line input to the Controller	Protected by internal 100 mA, 20 mm fuse. The phase-detected current is locked to the Controller supply voltage.
N	Supply neutral	

To replace the internal fuse, the rear cover must be removed.

2.4. Current Transformer Connection

The Controller uses a standard 5 A secondary current transformer (CT) to detect line or load current. The connection is effected at the power terminal block as follows:

Current Transformer Circuit Connection		
Terminal	**Connection**	**Comments**
C1	CT secondary current in	Detected across a 0.05 Ω sensing resistor.
C2	CT secondary current return	

The CT ratio is set as a separate Controller configuration parameter (3.6.3.1, p16).

2.5. Bit Input Connection

The Controller inputs are NPN (current sink) type. They are internally connected to the galvanically isolated internal interface power supply and are protected against overvoltage transients. The connection of the bit inputs is made at the signal terminal block as follows:

Bit Input Connection		
Terminal	**Connection**	**Comments**
I0	Enable Input 0	10 - 15 mA current signal.
I1	Enable Input 1	10 - 15 mA current signal.
I2	Enable Input 2	10 - 15 mA current signal.
I3	Enable Input 3	10 - 15 mA current signal.
I4	Enable Input 4	10 - 15 mA current signal.
I5	Enable Input 5	10 - 15 mA current signal.
I6	Enable Input 6	10 - 15 mA current signal.
I7	Enable Input 7	10 - 15 mA current signal.
I8	Enable Input 8	10 - 15 mA current signal.
I9	Enable Input 9	10 - 15 mA current signal.
I10	Enable Input 10	10 - 15 mA current signal.
I11	Enable Input 11	10 - 15 mA current signal.
IR	Input common	Interface power supply reference and signal return in three terminal positions.

For typical connection to optotransistors, relay/switch contacts and small sensors consult the wiring diagrams in Appendix B, p39.

2.6. Bit Output Connection

The Controller bit outputs feature 24 VDC optotransistors commoned in NPN (current sink) type. They are protected against overvoltage transients and are isolated from all other Controller supply potentials. The connection of the bit outputs is made at the signal terminal block as follows:

Bit Output Connection		
Terminal	**Connection**	**Comments**
O0	Output 0	20 mA current signal
O1	Output 1	20 mA current signal
O2	Output 2	20 mA current signal
O3	Output 3	20 mA current signal
O4	Output 4	20 mA current signal
O5	Output 5	20 mA current signal
O6	Output 6	20 mA current signal
O7	Output 7	20 mA current signal
O8	Output 8	20 mA current signal
O9	Output 9	20 mA current signal
O10	Output 10	20 mA current signal
O11	Output 11	20 mA current signal
OR	Output common	Isolated return in three terminal posistions

For typical connection to PLCs, relays and capacitor bank switches consult the wiring diagrams in Appendix B, p39.

2.7. RS232 Serial Port Connection

The RS232 port connection is effected at the signal terminal block as follows:

RS232 Serial Port Connection		
Terminal	**Connection**	**Comments**
TX	Data transmit, output	Short circuit protected
RX	Data receive, input	Overvoltage protection
NR	Signal reference	Common with RS485 port power supply

A PC port connection is made as follows:

PC Port Connection		
Signal	**D25 pin, PC**	**D9 pin, PC**
TX	3	2
R	7	5
RX	2	3

Some PCs may require the self-excitation of the hardware control signals. This can be done by shorting pins 4-5-6-8 at the D25 connector or 1-6-7-8 at the D9 one.

2.8. RS485 (Quamatic or similar) Network Connection

The RS485 network connection is effected by wiring all the network members to a common 2-wire (ideally shielded) cable. The cable should not have any branches (pure multidrop connection) and should be terminated at the two ends with 120 Ohm resistors.

The RS485 port is powered by the internal RS485/RS232 power supply and is galvanically isolated from the rest of the Controller circuits.

The connection is made as follows:

Quamatic RS485 Network Connection		
Terminal	**Connection**	**Comments**
N+	Positive signal	
NS	Shield connection	Port ground/reference
N-	Negative signal	

The 120 Ohm termination may be connected at the signal points N+ and N-.

3. PARAMETER PROGRAMMING

3.1. Overview

The Controller parameters can be programmed locally (via the front panel switches) and/or the serial ports (RS232 and RS485).

Local parameter programming is organized in a three-level menu structure grouped as summarized by the table:

Controller Parameter Menu Groups	
Parameter Group	**Group Members Description**
OPrtn	Overall Controller operation parameters
CAPS	Capacitor bank parameters
SEtuP	Installation and setup I/O, control, net, ADC, timing, user and service parameters

Parameters are organized under each group in menus and further submenus if necessary. Each is described in the following chapters.

All parameters can be set at any time while the Controller is powered. In this way the Controller operation can be determined dynamically (as in the case of fuzzy control).

Displayed parameter names and values are shown as they appear on the Controller display in `mono` font as with `OPrtn`, `CAPS` and `SEtuP` above. Menu positions are shown in navigational step format of the menu entries separated by the "»" character. As such, the `Ed.tmo` parameter under the `OPrtn` menu group is referred to as "`OPrtn` » `Ed.tmo`".

3.2. Local Parameter Programming

The Controller parameters can be read and set locally by operating the front panel switches. The table summarizes the programming procedure (and operation):

Local Controller Parameter Programming			
Switch	**Normal Operation**	**Parameter Selection**	**Parameter Setting**
CTRL	Changes to parameter selection state.	Selects the displayed parameter, control record or group to read or set.	Sets the parameter to the displayed value and returns to the parameter selection state (if allowed).
START/STOP	Start/stop of normal operation.	Exit from the parameter selection state or current menu level.	Returns to the parameter selection state without changing the parameter.
UP	Ignored	Displays the next parameter, control record or group.	Increases the displayed value.
DOWN	Ignored	Displays the previous parameter, control record or group.	Decreases the displayed value.

When no parameter changes are allowed locally (`SEtuP` » `USEr` » `EbL.Ed` parameter, p19), the user can only read the parameter values by following the above sequences.

The parameter programming procedures are under a time-out specified by the `OPrtn` » `Ed.tmo` parameter (p8). If no switch is pressed for the specified time, programming is canceled at time-out.

When incrementing/decrementing real and integer values, the value changes logarithmically. The step is halved at every change between increasing and decreasing direction, thus converging at the required value very quickly.

3.3. Parameter Programming via the Network or Local PC

Parameter and calibration table programming can also be performed via the serial ports with the respective command (‘Load CNF’ - Appendix A.6, p27). This function is also available in all Quamatic network management software (e.g. BENQNODE.exe).

3.4. Setting the Controller Operation Parameters Group `OPrtn`

3.4.1. Operation Parameters Group Overview

The group handles the parameters associated with general Controller operation as follows:

Controller Operation Group Parameters	
Parameter	**Description**
`diSPL`	Displayed variable.
`Ed.tmo`	Configuration parameter editing time-out.
`Sho.St`	Show disabled input status message with displayed variable.
`run`	Automatic start of operation after power-up.
`qt.Err`	Go Quiet after error.

3.4.2. Setting the Displayed Variable Group OPrtn » diSPL

While in normal operation, the Controller displays the various magnitudes specified by this parameter as follows:

Displayed Magnitude Index Parameter		
Value	**Description**	**Units, Comments**
SttuS	State and status messages	Displays system status or error condition.
LnE.PF	Line side power factor	
Lne.VA	Line side apparent power	In KVA
Ln.VAr	Line side reactive power	In KVAr
Lod.PF	Load side power factor	
Lod.VA	Load side apparent power	In KVA
Ld.VAr	Load side reactive power	In KVAr
PowEr	Load active power	In KW
Perod	Line period	In µs
Freq	Line frequency	In Hz
CAP.VA	Sum of connected capacitor size	In KVAr
CAP.Pc	Sum of connected capacitor size as a percentage of total bank size	In %
Aprt.C	Apparent current magnitude	In A
Actv.C	Active current magnitude	In A
rctv.C	Reactive current magnitude	In A
Ap.Adc	Apparent current ADC reading	In internal absolute units
Ph.Adc	Phase detected current ADC reading	In internal absolute units
S.timE	Local time	In HH.MM.S format
S.dAtE	Local date	In DD.MM.Y format
bit.In	Controller bit inputs	Displayed as three hex nibbles.
bit.oP	Controller bit outputs	Displayed as three hex nibbles.
Inp<NN>	Bit input NN (0..11) state	Displayed as "i<NN>.on/oF"
OutP<N> or Out<NN>	Bit output NN (0..11) state	Displayed as "o<NN>.on/oF". Output11 state is displayed as "oP.rdy/oP.Err" when assigned as a "Ready" output to an external master and "Fan.on/oF" when driving a ventilation fan.
incr	Panel Up switch	Displayed as "SiU.on/oF"
dEcr	Panel Down switch	Displayed as "Sid.on/oF"
StArt	Panel Start/Stop switch	Displayed as "SiS.on/oF"
CntrL	Panel Ctrl switch	Displayed as "SiC.on/oF"
SinPS	Panel switch state	Switches are shown by "S", "C", "u", "d" in the active state and by "_" when inactive.

Parameters SEtuP » Adc » rAtio (p16), SEtuP » Adc » UA.Ftr (p16) and SEtuP » Adc » A.Fctr (p16) must first be correctly set before any variable is shown in KW, KVA and KVAr.

3.4.3. Setting the Configuration Editing Time-out OPrtn » Ed.tmo

This parameter sets the maximum idle time between configuration editing commands in seconds.

When zero, no editing time-out is applied.

3.4.4. Setting the Status Messages with Displayed Variable Parameter OPrtn » Sho.St

This parameter enables the displaying of disabled input message dSb.in (p23) interleaved with the selected variable of Oprtn » diSPL (p8) as follows:

Status/Error Messages with Displayed Variable Parameter	
Value	**Description**
no.Sho	No message is shown interleaved with the display of a variable.
Show	Disabled input message dSb.in is shown interleaved with variable display at 0.5 Hz when a capacitor bank is disabled by its associated bit input, typically by a blown fuse or phase fault in the bank circuit.

3.4.5. Setting the Start of Operation Parameter OPrtn » run

This parameter enables the automatic starting of the Controller operation after reset as follows:

Start of Operation Parameter	
Value	**Description**
MAn.rn	After checking the parameters for integrity, the Controller is placed in “Quiet” mode waiting for the manual “Start” command (Start/Stop panel switch, if allowed by SEtuP » USEr » IGn.OP, p19) or the network “Go” command (p26).
Aut.rn	After checking the parameters for integrity, Controller operation begins automatically.

3.4.6. Setting the Quiet on Error Parameter OPrtn » qt.Err

This parameter forces the Controller to stop operating (go Quiet) in the event of a recoverable or non-recoverable error as follows:

Quiet on Recoverable Error Values	
Value	**Description**
EnbLE	The Controller goes in the Quiet state without attempting to recover or restart operation in the event of a fault or error.
dSbLE	The Controller recovers from fault/errors when their cause is removed or reboots after a non-recoverable error.

3.5. Capacitor Bank Characteristics Handling Group CAPS

The group organizes capacitor bank size and minimum discharge time as a submenu for each capacitor bank (CAPS » CAP 0 .. CAPS » CAP11) as follows:

Capacitor Bank CAPS » CAP<NN> Submenu Parameters	
Parameter	**Description**
CAP.V.<N> or CP.V.<NN>	Capacitor bank size in KVAr.
dSCh.<N> or dCh.<NN>	Capacitor bank discharge time in seconds. After switch-off, the bank will not be connected back to the line for at least this time.

Parameters SEtuP » Adc » rAtio (p16), SEtuP » Adc » UA.Ftr (p16) and SEtuP » Adc » A.Fctr (p16) must first be correctly set before any bank size is entered.

3.6. Setup and Installation Parameter Group SEtuP

The group organizes setup/installation parameters in bit I/O, control, net, ADC, timing, user and service submenus:

Controller Setup and Installation Group Submenus	
Submenu	**Description**
bit.io	Active low flags for the Controller bit inputs and outputs
CntrL	Control operation parameters
nEt	Serial communication parameters
Adc	Analog/Digital converter parameters
oPtn.t	Operation timing parameters
USEr	User/operator permissions
SErvc	System information and maintainance jobs

3.6.1. Setting the Parameters of the SEtuP » bit.io Submenu

This submenu organizes the active low flags of the Controller bit inputs and outputs:

Bit I/O Submenu Parameters	
Parameter	**Description**
A.Lo.IH	Active low flags for bit inputs 8..11
A.Lo.IL	Active low flags for bit inputs 0..7
A.Lo.OH	Active low flags for bit outputs 8..11
A.Lo.OL	Active low flags for bit outputs 0..7

The active low flags allow for individual inputs and outputs to interface to reverse logic sources or loads.

While in reset and up to the initial loading of the Controller parameters, all outputs are electrically deactivated.

The parameter value (0..255 or 0..15) is determined by adding the weights for each input or output which is of active-low type as follows:

Bit Input and Output Active-low Parameter Value		
Bit Input or Output 0..7	**Bit Input or Output 8..11**	**Weight Value to Add**
0	8	1
1	9	2
2	10	4
3	11	8
4		16
5		32
6		64
7		128

3.6.2. Submenu `SEtuP` » `CntrL` Parameters

This submenu organizes all control related parameters as follows:

Control Submenu Parameters	
Parameter	**Description**
`Ct.Inv`	Inverts current transformer (CT) polarity.
`In0.En`	Assign Bit Input 0 as a master enable input.
`En.rdy`	Assign Bit Input 11 and Bit Output 11 to interface to an external master.
`FAn.oP`	Assign Bit Output 11 to drive a fan.
`FAn.Ac`	Fan output activation limit in connected bank KVAr total
`PhASE`	Single- or three- phase line system
`CPtn.F`	Compensation factor value
`C.tYPE`	Control function type
`SYnch`	Ignore unsynchronized system time error.

3.6.2.1. Setting the `SEtuP` » `CntrL` » `Ct.Inv` Parameter

The Controller detects the reactive current of an inductor as positive and that of a capacitor as negative in polarity. This parameter inverts the detected current polarity logically to avoid physically swapping the CT connections in case inductive current is detected negative.

It is set as follows:

Invert Current Transformer (CT) Polarity Values	
Value	**Description**
`FoLo`	The detected current is not inverted in polarity.
`invrt`	The detected current is inverted in polarity.

The polarity of the detected current can be displayed by seting the `OPrtn` » `diSPL` parameter (p8) to `rctv.C` and detecting a known inductive or capacitive load.

3.6.2.2. Setting the `SEtuP` » `CntrL` » `In0.En` Parameter

Each Controller output uses it´s associated input as an external enable signal, typically supplied by a temperature sensor or similar device to signal that the specific capacitor bank is ready for use. This parameter specifies Bit Input 0 as a master enable signal to replace the individual enabling ones.

It is set as follows:

Bit Input 0 Assigned as a Master Enable Parameter Values	
Value	**Description**
`EnbLE`	Bit Input 0 is a master enable input replacing the individual capacitor bank enable inputs which are ignored.
`dSbLE`	Each capacitor bank is individually enabled by its associated input.

This parameter acts independently from the `SEtuP` » `CntrL` » `En.rdy` parameter (p12).

3.6.2.3. Setting the `SEtuP` » `CntrL` » `En.rdy` Parameter

The Controller can be interfaced to an external master device by employing the Bit Input 11 and Bit Output 11 pair to receive the enable command and return a "Ready" status output. This parameter specifies this as follows:

Bit 11 Pair Interface to a Master Parameter Values	
Value	**Description**
`EnbLE`	Bit Input 11 accepts an external enable input and Bit Output 11 is a "Ready" status output, subject to `SEtuP` » `CntrL` » `FAn.oP` (p13).
`dSbLE`	Bit I/O 11 is not interfaced to an external master device.

When disabled, the Controller continues operating normally (taking measurements, calculating and displaying variables) but does not activate the capacitor bank outputs.

The parameter acts independently from the `SEtuP` » `CntrL` » `In0.En` parameter (p12). When both parameters are enabled, the Controller banks are disconnected with either Bit Input 0 or Bit Input 11 disabled.

When this parameter is enabled and Bit Output 11 is also assigned to drive a fan (`SEtuP` » `CntrL` » `FAn.oP` parameter, p13), Bit Input 11 is effectively used as a second master enable input.

3.6.2.4. Setting the SEtuP » CntrL » FAn.oP and SEtuP » CntrL » FAn.Ac Parameters

The Controller can employ Bit Output 11 to control a ventilation fan when the connected capacitor bank total is above a given value. The facility is set as follows:

Bit Output 11 Fan Control Parameter Values	
Value	**Description**
no.FAn	Bit Output 11 does not control a fan.
FAn.Ct	Bit Output 11 drives a fan when the connected bank total is above the SEtuP » CntrL » FAn.Ac limit.

This parameter ignores and overides an enabled SEtuP » CntrL » En.rdy parameter (p12).

The fan activation limit is provided by the SEtuP » CntrL » FAn.Ac parameter in KVAr. Parameters SEtuP » Adc » rAtio (p16), SEtuP » Adc » UA.Ftr (p16) and SEtuP » Adc » A.Fctr (p16) must first be correctly set before any values are entered in KVAr.

3.6.2.5. Setting the SEtuP » CntrL » PhASE Parameter

This parameter determines if the phase-detected current is the active or reactive one. The Controller calculates the out-of-phase (or quadratue) component from the measured absolute (apparent) and phase-detected currents and, based on this parameter, sets the applicable active and reactive magnitudes.

The parameter is set as follows:

Phase System Parameter Values	
Value	**Description**
3-Ph	The Controller operates in a three-phase line system. The measured in-phase current is the reactive component and the calculated quadrature current is the active one.
1-Ph	The Controller operates in a single-phase line system. The measured in-phase current is the active component and the calculated quadrature is the reactive component.

The wiring of three-phase and single-phase installations is shown in Appendix B (p39).

3.6.2.6 Setting the compensation factor SEtuP » CntrL » CPtn.F parameter

The parameter sets the Controller to over- or under- compensate the detected inductive current so that either some inductance is left in the system ensuring line stability or when extra compensating capacitance is needed.

It is set as a value between 0.004 and 99.996.

3.6.2.7. Setting the `SEtuP` » `CntrL` » `C.tYPE` Parameter

The parameter sets the Controller to operate in compensating or regulating mode. It is set as follows:

Phase System Parameter Values	
Value	**Description**
`Ld.Sd.C`	The Controller detects current on the load side and operates in compensating mode. In this mode the Controller switches the banks in and out of the line to compensate the detected reactive load current as closely as feasible by the available bank sizes and subject to the `SEtuP` » `CntrL` » `CPtn.F` parameter (p13).
`Ln.Sd.r`	The Controller detects current on the line side and opeartes in regulating mode. In this mode the Controller switches capacitor banks in and out of the line to minimize reactive current at the line side subject to the `SEtuP` » `CntrL` » `CPtn.F` parameter (p13). Using this mode is not possible in single-phase installations (3.6.2.5, p13 above).

3.6.2.8. Setting the Always Synchronized `SEtuP` » `CntrL` » `SYnch` Parameter

The Controller system time and date are initialized as zero at power-up and reported as unsynchronized until set by a "Synchronization command" (Appendix A.9, p28) via the serial ports. This feature is not required when the Controller is operating on its own and this parameter enables it as follows:

Ignore Unsynchronized Status Parameter Values	
Value	**Description**
`EnbLE`	Ignores unsynchronized status/error.
`dSbLE`	Reports unsynchronized status/error.

3.6.3. Submenu `SEtuP` » `nEt` Parameters

This submenu organizes all serial port and network related parameters as follows:

Network Submenu Parameters	
Parameter	**Description**
`bAUd`	Sets the port baud rate.
`AdrES`	Sets the Controller network address/identity.
`nEt.to`	Net activity time-out
`n.cd.to`	Net command activity time-out
`Eor.ch`	Extra XOR checksum byte

3.6.3.1. Setting the Baud Rate `SEtuP` » `nEt` » `bAUd` Parameter

This parameter specifies the serial port communication speed.

3.6.3.2. Setting the Baud Rate `SEtuP` » `nEt` » `AdrES` Parameter

This parameter specifies the Controller address in the network. The valid range of values is 1..255 with 0 being reserved for broadcasted messages to all members of the network.

3.6.3.3. Setting the Net Activity Time-out `SEtuP` » `nEt` » `nEt.to` Parameter

This parameter specifies in seconds the maximum time for any message to be issued in the network. On time-out the `Er.Com` error is set.

When set to zero, the facility is disabled.

3.6.3.4. Setting the Net Command Time-out `SEtuP` » `nEt` » `ncd.to` Parameter

This parameter specifies in seconds the maximum time for any command to be received by the Controller from the network. On time-out the `Er.Cmd` error is set.

When set to zero, the facility is disabled.

3.6.3.5. Setting the Extra XOR Checksum Byte `SEtuP` » `nEt` » `Eor.ch` Parameter

This parameter checks the extra XOR checksum byte in the exchanged Quamatic messages as follows:

Extra XOR Quamatic Checksum Values	
Value	**Description**
`EnbLE`	The extra XOR checksum byte is expected in the received Quamatic messages and included by the Controller when sending a message.
`dSbLE`	No extra XOR checksum is expected or checked by the Controller. However, in versions v0r2 and above, one is included in all transmissions.

3.6.4. Submenu `SEtuP` » `Adc` Parameters

This submenu organizes all analog measurement and conversion parameters as follows:

Analog Measurement and Conversion Submenu Parameters	
Parameter	**Description**
`rAtio`	Sets current transformer (CT) primary/secondary ratio.
`UA.Ftr`	Sets the A to KVA conversion factor.
`A.Fctr`	Sets the ADC units to A conversion factor.
`qd.SGn`	Sets the sign of the calculated quadrature current.
`Ab.oFS`	Sets the absolute (apparent) current measurement offset in ADC units.
`Ph.oFS`	Sets the phase detected (active or reactive) current measurement offset in ADC units.
`ZEro`	Loads current absolute and phase detected ADC readings as offsets in `SEtuP` » `Adc` » `Ab.oFS` and `SEtuP` » `Adc` » `Ph.oFS` respectively.

3.6.4.1. Setting the CT Ratio `SEtuP` » `Adc` » `rAtio` Parameter

This parameter sets the current transformer primary to secondary ratio. When a 100/5 A transformer is used, the parameter value should be set equal to 20.

3.6.4.2. Setting the KVA Factor `SEtuP` » `Adc` » `UA.Ftr` Parameter

This parameter sets the factor to calculate all KW, KVA and KVAr variables and parameters from their associated current component in Amperes.

In three-phase installations it should be set to 1.732*V_L where V_L is the line voltage. In single-phase installations it should be set to the system phase voltage.

3.6.4.3. Setting the Ampere Factor `SEtuP` » `Adc` » `A.Fctr` Parameter

This parameter sets the factor to calculate all current variables and parameters in Amperes from their associated ADC units and is the only quantity needed to calibrate the Controller measurement gain. This parameter is part of the data saved in read-only space following factory calibration and loaded as defaults (3.6.7.7, p21).

The parameter must be set to 1/ADC_{1A} where ADC_{1A} is the ADC apparent reading – ADC apparent offset at 1 A secondary CT current.

Controller calibration is discussed in 3.6.4.7 below.

3.6.4.4. Setting the Quadrature Current Sign `SEtuP` » `Adc` » `qd.SGn` Parameter

This parameter sets the sign of the calculated quadrature, out-of-phase current. The quadrature current is calculated as √(apparent current squared – phase detected current squared) and can be set to take the sign of the in-phase current for diagnostic purposes.

This parameter is set as follows:

Quadrature Current Sign Values	
Value	**Description**
`PoStv`	The sign of the quadrature current is always positive. Used during normal operation.
`FoLo`	The sign of the quadrature current is the same with the phase detected one. Diagnostic use only.

3.6.4.5. Setting the Apparent Current Offset `SEtuP` » `Adc` » `Ab.oFS` Parameter

This parameter sets the ADC offset in the apparent current measurement. The offset is subtracted from the ADC reading to provide the apparent current magnitude in ADC counts. These parameters are part of the data saved in read-only space following factory calibration and loaded as defaults (3.6.7.7, p21).

The parameter can be automatically set by the `SEtuP` » `Adc` » `ZEro` procedure (3.6.4.7, below) and Controller calibration is discussed in 3.6.4.8 below.

3.6.4.6. Setting the Phase-Detected Current Offset `SEtuP` » `Adc` » `Ph.oFS` Parameter

This parameter sets the ADC offset in the phase-detected current measurement. The offset is subtracted from the ADC reading to provide the phase-detected current magnitude in ADC counts.

The parameter can be automatically set by the `SEtuP` » `Adc` » `ZEro` procedure (3.6.4.7, next) and Controller calibration is discussed in 3.6.4.8 below.

3.6.4.7. Automatic Offset Setting `SEtuP` » `Adc` » `ZEro` Procedure

The procedure loads the current ADC apparent and phase-detected readings to the respective offset parameters `SEtuP` » `Adc` » `Ab.oFS` and `SEtuP` » `Adc` » `Ph.oFS` (3.6.4.5 and 3.6.4.6 above).

3.6.4.8. Controller Calibration Procedure

Controller calibration is made in two steps. First the ADC offsets are measured and then the system current gain is determined.

With no current through the CT, the ADC absolute and phase-detected channel offsets are taken and saved to the `SEtuP` » `Adc` » `Ab.oFS` and `SEtuP` » `Adc` » `Ph.oFS` parameters (p16) respectively. This can be done manually by displaying the reading of each channel after setting the `OPrtn` » `diSPL` parameter (p8) to `AP.Adc` and `Ph.Adc` respectively. Alternativelly, the automatic offset setting procedure `SEtuP` » `Adc` » `ZEro` (p17) may be used.

The measurement gain is determined by passing known (up to 5 A) secondary CT current through the Controller and observing the apparent current ADC reading. The gain is calculated after subtracting the relevant ADC channel offset and saved in the `SEtuP` » `Adc` » `A.Fctr` parameter (p16).

3.6.5. Submenu SEtuP » oPtn.t Parameters

This submenu organizes all Controller timing parameters as follows:

Controller Timing Submenu Parameters	
Parameter	**Description**
Av.Prd	Sets the Controller averaging period during which ADC samples are accumulated.
idL t	Sets the minimum idle time the Controller must spend after going Quiet.
S.idL.t	Sets the time between switching individual capacitor banks.
L.Prd.S	Sets the number of line period samples to average in line frequency/period measurement.

3.6.5.1. Setting the Controller Averaging Period SEtuP » oPtn.t » Av.Prd Parameter

The parameter sets the Controller averaging period in seconds.

During this period the Controller accumulates ADC samples to calculate the average values for the apparent and phase-detected currents.

3.6.5.2. Setting the Controller Idle Time SEtuP » oPtn.t » idL t Parameter

The parameter sets the Controller idle time in seconds.

This idle time is spent as a minimum, with the banks off, following an error, fault or reboot to avoid any destabilizing bank switching during line faults or system errors.

3.6.5.3. Setting the Switch Idle Time SEtuP » oPtn.t » S.idL.t Parameter

The parameter sets the minimum switch idle time in seconds.

This idle time is spent between individual bank switching so that capacitor banks are switched in or out of the line one at a time and should be at least set to the bank switch response time.

3.6.5.4. Setting the Line Period Sample Size SEtuP » oPtn.t » L.Prd.S Parameter

The parameter sets the number of line period samples to average in measuring the line period and frequency.

3.6.6. Submenu SEtuP » USEr Parameters

This submenu organizes user permissions as follows:

Controller User Submenu Parameters	
Parameter	**Description**
iGn.OP	Set to ignore operator Start/Stop commands.
EbL.Ed	Shows if configuration parameter editing is allowed.

3.6.6.1. Setting the "Ignore Operator" SEtuP » USEr » iGn.OP Parameter

This parameter disables the Start/Stop operator command as follows:

"Ignore Operator" Parameter	
Value	**Description**
LiStn	Allows for the operator to start and stop operation via the Start/Stop front panel switch.
Ignor	Ignores Start/Stop commands from the front panel.

The SEtuP » USEr » iGn.OP parameter acts independently from the SEtuP » USEr » EbL.Ed parameter (p19) and can be changed via the “Load CNF” command from the net (Appendix A.6, p27).

3.6.6.2. Displaying the Enable Parameter Editing SEtuP » USEr » EbL.Ed Value

The parameter enables parameter editing by the operator as follows:

Enable Parameter Editing Parameter	
Value	**Description**
EnbLE	Allows the operator to edit the Controller parameters via the front panel switches.
dSbLE	Ignores any parameter changes from the panel switches. Only viewing of the parameter values is allowed.

All Controller parameters can be changed, regardless of the SEtuP » USEr » EbL.Ed value, from the network (“Load CNF” command, Appendix A.6, p27). The SEtuP » USEr » EbL.Ed parameter can also be set/reset with the SEtuP » SErvc » LocEd and SEtuP » SErvc » UnLoc procedures (p20).

3.6.7. Submenu **SEtuP** » **SErvc** Parameters

This submenu organizes all service/maintainance parameters and procedures as follows:

Service Submenu Parameters	
Parameter	**Description**
VErSn	Shows Controller software version.
tYPE	Shows Controller hardware type.
CLr.Er	Clears all errors.
Er.Src	Shows source of internal processing error Er.Prc
LocEd	Locks parameter editing.
UnLoc	Unlocks parameter editing.
L.dFLt	Loads parameter default.

3.6.7.1 Displaying the Controller Software Version SEtuP » SErvc » VerSn value

This menu entry shows the Controller software version and release.

3.6.7.2. Displaying the Controller Hardware Type SEtuP » SErvc » tYPE Value

This menu entry shows the Controller hardware group and platform type.

3.6.7.3. Clear All Errors SEtuP » SErvc » Clr.Er Procedure

This procedure clears all Controller errors and the SEtuP » SErvc » Er.Src source.

3.6.7.4. Show Source of Internal Error SEtuP » SErvc » Er.Src Procedure

This procedure shows the source of the last internal processing error.

3.6.7.5. Lock Parameter Editing SEtuP » SErvc » LocEd Procedure

This procedure disables parameter editing via the Controller front panel by clearing the SEtuP » USEr » EbL.Ed parameter (p19).

3.6.7.6. Unlock Parameter Editing `SEtuP` » `SErvc` » `UnLoc` Procedure

This procedure enables parameter editing via the Controller front panel by setting the `SEtuP` » `USEr` » `EbL.Ed` parameter (p19).

3.6.7.7. Load Parameter Defaults `SEtuP` » `SErvc` » `L.dFLt` Procedure

This procedure loads the Controller parameters with their default values.

The ADC absolute and phase-detected channel offset and current gain parameters are copied from the read-only factory calibration data. They are saved to the `SEtuP` » `Adc` » `Ab.oFS` and `SEtuP` » `Adc` » `Ph.oFS` parameters (p16) and `SEtuP` » `Adc` » `A.Fctr` (p16) respectively.

4. CONTROLLER OPERATION

4.1. Controller Operation Overview

On power up the Controller checks the integrity and valid operational state of the various subsystems and, depending on the value of the `OPrtn » run` (p9) parameter, waits for the manual or network command to start operation or begins according to the parameter values. The command can originate from the operator (Start/Stop panel switch, if allowed by `SEtuP » USEr » iGn.OP`, p19) or from the network/serial port ("Go" command, p26).

Normal operation can be stopped manually (Start/Stop panel switch, if allowed by `SEtuP » USEr » iGn.OP`, p19) or via the network/serial port ("Quiet" command, p26). While in Quiet state, the outputs are logically deactivated with their electrical state determined by the `SEtuP » bit.io » A.Lo.OH` and `SEtuP » bit.io » A.Lo.OL` parameters (p10).

While in normal operation, the Controller reads the line period, the bit inputs and the apparent and phase-detected currents, averages them and calculates the active and reactive components as well as all derived quantities. Following this and depending on the control mode and other parameter values the outputs are driven in regulating or compensating mode.

Capacitor banks are always switched largest first and one at a time as specified by the `SEtuP » oPtn.t » S.idL.t` parameter (p18). Banks are not switched in when they are discharging as specified by their associated `CAPS » CAP<NN> » dSCh.<N>/dCh.<NN>` parameter (p10). Current measurement is suspended during bank switching to exclude any transient effects.

The display shows the variable specified by the `OPrtn » diSPL` parameter (p8) and may be interleaved with a `dSb.in` message (p23) if any bank is disabled at the Controller bit inputs. (The `dSb.in` message is not interleaved with parameter `OPrtn » Sho.St` disabled (p9), in which case it can only appear when the `OPrtn » diSPL` parameter is set to `SttuS`). The right-most decimal point of the display is flashed at every sampling instant while displaying variables.

In the case of an error or fault condition, the Controller enters the idle state (banks are turned off) and displays the associated error message. The Controller may recover (if allowed by the `OPrtn » qt.Err` parameter, p9) when the cause is removed or reboots if not successful. If the error condition persists or another one occurs, the Controller will again display the associated error message and wait to recover or reboot.

4.2. Controller Error Handling

The Controller outputs are placed in their idle state while in the error state and the Controller will reboot when recovery is not possible.

A recoverable error state is cleared:

- when its cause is removed, or
- by acknowledging it manually by pressing the Ctrl panel switch, or
- by the “ZeroError” network command (p29) or the `SEtuP` » `SErvc` » `Clr.Er` procedure (p20).

The table summarizes the various Controller status and error messages, their causes and Controller actions:

Controller Status and Error Messages	
Message	**Description**
`- - - - -`	Bad parameter values. Requires setting of all configuration parameters. In most cases default values will be automatically loaded. If not, they can be loaded manually with the `SEtuP` » `SErvc` » `L.dFLt` procedure (p21).
`. . . . .`	Quiet state. The message is flashed while banks are turned off one at a time following a command or error to enter the Quiet state.
`Er.Sav`	Error in parameter saving or bad memory. The Controller cannot recover and reboots. The error can be cleared by the `SEtuP` » `SErvc` » `Clr.Er` procedure (p20).
`Er.Prc`	Internal processing error caused by numerical overflow or other similar cause. The Controller cannot recover and reboots. The error can be cleared by the `SEtuP` » `SErvc` » `Clr.Er` procedure (p20) and its source can be displayed by the `SEtuP` » `SErvc` » `Er.Src` procedure (p20).
`Er.Com`	Net activity time-out. The Controller goes idle and waits for the error to be cleared by any activity in the network or a user command. Enabled by the `SEtuP` » `nEt` » `nEt.to` parameter (p15).
`Er.Cmd`	Net command time-out. The Controller goes idle and waits for the error to be cleared by a new net or a user command. Enabled by the `SEtuP` » `nEt` » `ncd.to` parameter (p15).
`Er.Src` or `Er.Out`	Bad line voltage input. The errors are caused by the line frequency being outside the 45-65 Hz range, typically caused by line faults or distortion. The Controller goes idle and waits for the error to be cleared by a clean line or a user command.
`no.tmE`	No time set. The Controller continues to operate normally. The error clears when a "Synchronization" command is received and can be disabled with the `SEtuP` » `CntrL` » `SYnch` parameter (p14).
`nEt.Er`	Net error while receiving a net message, typically caused by wrong baud rate, bad checksum or noise in the network. The Controller ignores the message and continues operating normally but may time-out if the net activity `SEtuP` » `nEt` » `nEt.to` or net command `SEtuP` » `nEt` » `ncd.to` parameters (p15) are enabled.
`dSb.in`	Disabled input status message shown when a capacitor bank is disabled by its associated bit input, typically indicating a fault in the capacitor bank circuits. The message may be set to be interleaved with the displayed variable via the `OPrtn` » `Sho.St` parameter (p9).
`dF.CnF`	Default values have been loaded manually, automatically or by a net command. To acknowledge and clear it, the Ctrl panel switch must pressed.
`idLE`	Idle status message shown when displaying power factor variables and no current is detected.
`rEAdy`	Ready status message shown when no banks are activated.
`no.Err`	No error status message shown when a number of banks are activated.

APPENDIX A. SERIAL DATA COMMUNICATION

A.1. Overview

Communications always start with a command to the addressed Controller. The command can be issued from software running on a PC or any other serial data source. The Controller responds with a relevant message.

All exchanged messages have the following format ('double DLE'):

```
<DLE><STX> <COMMAND> <DATA> <XORCHKSUM> <CHECKSUM> <DLE><ETX>
```

where `<DLE>` is the ASCII 'Data Link Escape' character (hex 16), `<STX>` is the ASCII 'Start of TeXt' character (hex 2), `<COMMAND>` represents the command characters, `<DATA>` represents the exchanged data bytes (if present), `<XORCHKSUM>` and `<CHECKSUM>` are checksum bytes of the message characters and `<ETX>` is the ASCII 'End of TeXt' character (hex 3). When a byte in the message block (`<COMMAND><DATA><XORCHKSUM><CHECKSUM>`) has the value `<DLE>` it is repeated (i.e. it is transmitted as `<DLE><DLE>`), so that the message opening string (`<DLE><STX>`) and the message closing string (`<DLE><ETX>`) are unique.

In this way, upon arrival of the sequence `<DLE><STX>`, the receiver prepares for the reception of a new message (network command or Controller response). Upon reception of a `<DLE><DLE>` pair only one character `<DLE>` is kept and message reception is concluded with the arrival of the sequence `<DLE><ETX>`. Message processing starts immediately after the arrival of the message closing sequence. The XOR checksum byte (`<XORCHKSUM>`) is equal to XORing the message bytes sequentially and the second checksum byte (`<CHECKSUM>`) is equal to the simple sum (ignoring any generated carry) of the message body `<COMMAND><DATA><XORCHKSUM>`. The XOR checksum may not be present if disabled by the `SEtuP` » `nEt` » `Eor.ch` parameter.

The command sequence `<COMMAND>` contains the identifying address byte `<ADRS>` of the commanded or responding station. Thus, the Controller only responds to commands addressed to it (specified by the `SEtuP` » `nEt` » `AdrES` parameter) and includes its identity in all its responses.

Broadcasting messages are characterized by a zero command address and the message is received by all members of the network. In this case the Controller responds only locally at the RS232 port.

Like all other Quamatic hardware, the Controller processes data with the most significant byte first.

The table summarizes the available Controller commands:

Controller Commands	
Command	**Description**
Status	Requests the Controller status.
Go	Starts normal operation.
Quiet	Suspends normal operation and turns to the Quiet state.
Configuration	Requests Controller parameters.
Load Configuration	Loads new parameters to the Controller.
Progress	Requests progress data from the Controller.
Fix variables	Sets the bank outputs, the XOR checksum flag and calibration data.
Set time	Synchronizes the Controller clock (current time and date)
Who Are You	Asks the Controller hardware and software characteristics
Zero/Clear variables	Clears the bank discharge counts, errors and net command flag.
Initialize/reboot	Reboots the Controller.
XOR checksum flag	Sets, clears or reports the state of XOR checksum enable flag.
Echo message	Transmits received message.

A.2. Status Command

The command message consists from the sequence `<ADRS>'S'`.

The Controller responds by the string:

```
<ADRS> <status>
```

where `<status>` is the current status value.

The possible values are:

Status Byte or Error Code Values	
Value	**Description**
0	OK, no error
3	Controller cold-booted, reported once.
4	Controller warm-booted, reported once.
5	No valid Controller parameters
6	Controller in Quiet state
7	New Controller parameters (from the operator/front panel)
8	Controller system time and date are not set
9	Unknown hardware error
10	Error in serial communication
11	Command parsing error
12	Unimplemented/unknown command
13	System booted after watchdog reset, reported once.
14	System reboots after non-recoverable error.
15	Net communication time-out
16	Net command time-out
17	System rebooted successfully after non-recoverable error, reported once.
18	System reboot after low power, reported once.
19	System reboot after net command, reported once.
20	Bad display index
21	Out of range value
30	Bad input signal
32	Error in value processing. Status byte followed by error source word.
36	Command could not be executed

A.3. Go Command

The Go command starts the Controller normal operation.

It has the form `<ADRS>'G'`.

The Controller responds with a Status message.

A.4. Quiet Command

The Quiet command sets the Controller in the Quiet state.

It has the form `<ADRS>'Q'`.

The Controller responds with a status message.

A.5. Parameter (Configuration) Request Command

The command requests a number of the Controller parameters and has the form:

`<ADRS> 'C' <offset> <count>`

where `<offset>` is the position (a zero-based word value) of the first requested parameter and `<count>` is the number (word value) of the requested bytes.

The Controller responds with the sequence:

`<ADRS> <status> <data>`

where <data> represents the requested data. If an error occurs no data is sent.

The parameter (Configuration) block fields are given in A.15.1, p31.

A.6. Load Parameters (Load CNF) Command

The command loads new parameter values to the Controller. It has the form:

`<ADRS> 'L' <offset> <data>`

where `<offset>` is the position (zero-based word value) of the first byte in the parameter block and `<data>` is the sequence of the new values.

The Controller responds with a status message. If no error occurs, the configuration parameter checksum is recalculated and saved without any validity checks.

The parameter block fields are given in A.15.1, p31.

A.7. Progress Data Request

The command requests the current Controller progress data and has the form `<ADRS>'P'<type>`, where `<type>` specifies the requested record type.

The table summarizes the available progress record types:

Progress Record Types	
Type value	**Description**
'F'	Full progress record.
'T'	Controller system time and date record.
'B'	Controller bit I/O states.
'E'	Controller error data.
'H'	Controller hardware readings
'd'	Current discharge table.
'b'	Controller bank size table
'a'	Controller ADC readings

The Controller responds with the sequence:

`<ADRS> <status> <progress>`

where `<progress>` is the requested data. If an error occurs, no data is sent.

The progress record fields are given in A.15.2-A.15.9, p34.

A.8. Fix Variables Command

The command specifies operation variables which are not part of the configuration parameters record and has the form:

`<ADRS> 'F' <variable> <value>`

where `<variable>` specifies the variable and `<value>` is the value of the variable.

The table summarizes the available variables for this command:

Fix Command Variables	
<variable> Value	**Description**
'O'	Sets Bit Outputs 8-11. The Controller sets the internal Net Control flag and stops controlling the banks.
'o'	Sets Bit Outputs 0-7. The Controller sets the internal Net Control flag and stops controlling the banks.
'X'	Temporary set/clear of the XOR checksum activity.
'C'	Save ADC calibration data. Used once, following factory calibration.

The Controller responds with a Status message.

A.9. Synchronization Command

The command synchronizes the Controller clock (time and date) and has the form:

`<ADRS> 'T' <systime>`

where `<systime>` is a timestamp record.

The Controller responds with a Status message.

The timestamp record fields are given in A.15.8, p37.

A.10. Identity Request (Who Are You)

The command requests the Controller identity data and has the form `<ADRS><ENQ>`, where `<ENQ>` is the ASCII 'ENQuire' character (hex 5).

The Controller responds with the sequence:

`<ADRS> <status> <id>`

where `<id>` is the identity record containing the requested data.

The record fields are given in A.15.10, p38.

A.11. Zero/Clear Variables Command

The command zeroes or clears variables and has the form:

`<ADRS> 'Z' <type>`

where `<type>` specifies the variable to be cleared.

The table summarizes the available variables for this command:

Fix Command Variables	
<type> Value	**Description**
'n'	Clears the internal Net Control flag and the Controller starts controlling the banks.
'd'	Clears all bank discharge counts.
'E'	Clears all errors and the SEtuP » SErvc » Er.Src source.

The controller responds with a Status message.

A.12. Initialize/reboot Command

The command reboots and initializes the Controller and has the form:

`<ADRS> 'Init'`

The Controller responds with a Status message before rebooting.

A.13. XOR Checksum Flag Command

The command sets, clears or reports the XOR checksum activity flag and has the form:

`<ADRS> 'Xsum' <type>`

where `<type>` specifies the action to be taken.

The table summarizes the available options for this command:

Fix Command Variables	
<type> Value	**Description**
'S'	Sets the XOR checksum activity flag. The controller responds with a Status message.
'C'	Clears the XOR checksum activity flag. The controller responds with a Status message.
'V'	Reports the XOR checksum activity flag state. The Controller responds with the string `<ADRS><status><value>` where the `<value>` byte is zero for no XOR activity and =1 otherwise.

A.14. Echo Message Command

The command echoes/retransmits a received message and has the form:

`<ADRS> 'e' <message>`

where `<message>` is the message to be echoed.

The Controller responds with the string:

`<ADRS> <status> <message>`

A.15. Data Records and Field Symbol Values

A.15.1. Configuration Parameter Record

The configuration parameter record fields are given in the following table:

Controller Parameter (Configuration) Block Fields			
Field	**Offset, Bytes**	**Type**	**Description**
NET_ADRS	0	byte	Controller address (`SEtuP` » `nEt` » `AdrES`)
COMBAUD	1	byte	Communication Baud rate index (`SEtuP` » `nEt` » `bAUd`). 0: 75, 1: 110, 2: 150, 3: 300, 4: 600, 5: 1200, 6: 2400, 7: 4800, 8: 9600, 9: 14400, 11: 28800, 12: 37500, 15: 62500. Above 9600 is not practical for RS232 port
FUN_FLAGS	2	byte	Function bits/flags. b2: `OPrtn` » `qt.Err`, b3: `SEtuP` » `CntrL` » `SYnch`, b4: `SEtuP` » `nEt` » `Eor.ch`, b7: `OPrtn` » `run`
OPRTN_FLAGS	3	byte	Operation bits/flags. b0: `SEtuP` » `CntrL` » `PhASE`, b1: `SEtuP` » `CntrL` » `Ct.Inv`, b2: `SEtuP` » `CntrL` » `In0.En`, b3: `SEtuP` » `CntrL` » `En.rdy`, b4: `SEtuP` » `CntrL` » `FAn.oP`, b5: `OPrtn` » `Sho.St`, b6: `SEtuP` » `Adc` » `qt.SGn`
MENU_FLAGS	4	byte	Menu bits/flags. b1: `SEtuP` » `USEr` » `iGnOP`, b6: `SEtuP` » `USEr` » `EbL.Ed`.

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Controller Parameter (Configuration) Block Fields			
Field	**Offset, Bytes**	**Type**	**Description**
CNF_DURTN	5	byte	Configuration editing time-out (`OPrtn` » `Ed.tmo`)
COMS_TMOUT	6	byte	Net inactivity time-out (`SEtuP` » `nEt` » `nEt.to`)
NCMD_TMOUT	7	byte	Net command time-out (`SEtuP` » `nEt` » `ncd.to`)
BIN_ACLO_L	8	byte	Active low bit input 0-7 flags (`SEtuP` » `bit.io` » `A.Lo.IL`)
BIN_ACLO_H	9	byte	Active low bit input 8-11 flags (`SEtuP` » `bit.io` » `A.Lo.IH`)
BOP_ACLO_L	10	byte	Active low bit output 0-7 flags (`SEtuP` » `bit.io` » `A.Lo.OL`)
BOP_ACLO_H	11	byte	Active low bit output 8-11 flags (`SEtuP` » `bit.io` » `A.Lo.OH`)
CTRL_MODE	12	byte	Control mode (`SEtuP` » `CntrL` » `c.tYPE`). 0: Compensation, 1: Regulation.
KVA_MULT	13	word	KVA multiplier (`SEtuP` » `Adc` » `UA.Ftr`) fraction. KVA multiplier= KVA_MULT/65536.
SCUR_FCTR	15	long word	ADC ampere factor (`SEtuP` » `Adc` » `A.Fctr`). Ampere factor=SCUR_FCTR/65536.
ABS_CUR_OFST	19	word	Apparent channel ADC offset (`SEtuP` » `Adc` » `Ab.oFS`).
PHSD_CUR_OFST	21	word	Phase-detected channel ADC offset (`SEtuP` » `Adc` » `Ph.oFS`).
CAPBANK_0	23	word	Bank 0 size in ADC counts (`CAPS` » `CAP 0` » `CAP.V.0`).
CAPBANK_1	25	word	Bank 1 size in ADC counts (`CAPS` » `CAP 1` » `CAP.V.1`).
CAPBANK_2	27	word	Bank 2 size in ADC counts (`CAPS` » `CAP 2` » `CAP.V.2`).
CAPBANK_3	29	word	Bank 3 size in ADC counts (`CAPS` » `CAP 3` » `CAP.V.3`).
CAPBANK_4	31	word	Bank 4 size in ADC counts (`CAPS` » `CAP 4` » `CAP.V.4`).
CAPBANK_5	33	word	Bank 5 size in ADC counts (`CAPS` » `CAP 5` » `CAP.V.5`).
CAPBANK_6	35	word	Bank 6 size in ADC counts (`CAPS` » `CAP 6` » `CAP.V.6`).
CAPBANK_7	37	word	Bank 7 size in ADC counts (`CAPS` » `CAP 7` » `CAP.V.7`).
CAPBANK_8	39	word	Bank 8 size in ADC counts (`CAPS` » `CAP 8` » `CAP.V.8`).
CAPBANK_9	41	word	Bank 9 size in ADC counts (`CAPS` » `CAP 9` » `CAP.V.9`).
CAPBANK_10	43	word	Bank 10 size in ADC counts (`CAPS` » `CAP10` » `CP.V.10`).
CAPBANK_11	45	word	Bank 11 size in ADC counts (`CAPS` » `CAP11` » `CP.V.11`).

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Controller Parameter (Configuration) Block Fields			
Field	**Offset, Bytes**	**Type**	**Description**
DISCHRG_0	47	word	Bank 0 discharge time in Controller "ticks" (`CAPS` » `CAP 0` » `dSCh.0`).
DISCHRG_1	49	word	Bank 1 discharge time in Controller "ticks" (`CAPS` » `CAP 1` » `dSCh.1`).
DISCHRG_2	51	word	Bank 2 discharge time in Controller "ticks" (`CAPS` » `CAP 2` » `dSCh.2`).
DISCHRG_3	53	word	Bank 3 discharge time in Controller "ticks" (`CAPS` » `CAP 3` » `dSCh.3`).
DISCHRG_4	55	word	Bank 4 discharge time in Controller "ticks" (`CAPS` » `CAP 4` » `dSCh.4`).
DISCHRG_5	57	word	Bank 5 discharge time in Controller "ticks" (`CAPS` » `CAP 5` » `dSCh.5`).
DISCHRG_6	59	word	Bank 6 discharge time in Controller "ticks" (`CAPS` » `CAP 6` » `dSCh.6`).
DISCHRG_7	61	word	Bank 7 discharge time in Controller "ticks" (`CAPS` » `CAP 7` » `dSCh.7`).
DISCHRG_8	63	word	Bank 8 discharge time in Controller "ticks" (`CAPS` » `CAP 8` » `dSCh.8`).
DISCHRG_9	65	word	Bank 9 discharge time in Controller "ticks" (`CAPS` » `CAP 9` » `dSCh.9`).
DISCHRG_10	67	word	Bank 10 discharge time in Controller "ticks" (`CAPS` » `CAP10` » `dCh.10`).
DISCHRG_11	69	word	Bank 11 discharge time in Controller "ticks" (`CAPS` » `CAP11` » `dCh.11`).
SAMPLING_PRD	71	word	Current sampling/averaging period in Controller "ticks" (`SEtuP` » `oPtn.t` » `Av.Prd`).
IDLE_TIME	73	word	Idle time in Controller "ticks" (`SEtuP` » `oPtn.t` » `idL t`).
SWITCHNG_IDLE	75	word	Bank switching idle time in Controller "ticks" (`SEtuP` » `oPtn.t` » `S.idL.t`).
COMP_FCTR	77	word	Compensation factor (`SEtuP` » `CntrL` » `Cptn.F`). Compensation factor= COMP_FCTR/256
CT_RATIO	79	word	Current transformer ratio (`SEtuP` » `Adc` » `rAtio`)
FAN_BANK	81	word	Total bank size to activate fan output (`SEtuP` » `CntrL` » `FAn.Ac`) in ADC counts.
AVG_PSAMPLS	83	byte	Line period averaging samples (`SEtuP` » `oPtn.t` » `L.Prd.S`)
CONF_SUM	84	byte	Configuration block simple checksum

A.15.2. Full Progress Record

The full progress record fields are summarized in the following table:

Controller Full Progress Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
SYS_YEAR	0	integer	Current system year
SYS_MONTH	2	byte	Current system month
SYS_DATE	3	byte	Current system day
SYS_HRS	4	byte	Current system hour
SYS_MINS	5	byte	Current system minutes
SYS_SECS	6	byte	Current system seconds
BINH_FLGS	7	byte	Current bit input 8-11 logical state flags
BINL_FLGS	8	byte	Current bit input 0-7 logical state flags
BOPH_FLGS	9	byte	Current bit output 8-11 logical state flags
BOPL_FLGS	10	byte	Current bit output 0-7 logical state flags
NEXT_BOPH	11	byte	Scheduled bit output 8-11 logical state flags
NEXT_BOPL	12	byte	Scheduled bit output 0-7 logical state flags
DISCHRGH_FLGS	13	byte	Current bank 8-11 active discharge flags
DISCHRGL_FLGS	14	byte	Current bank 0-7 active discharge flags
USER_INFLGS	15	byte	Current switch input flags. b0: StArt/Stop, b1: Cntrl, b2: decr, b3: Incr.
ABS_CMEAS	16	word	Current apparent ADC channel count
PHD_CMEAS	18	word	Current phase-detected ADC channel count
SPRD	20	word	Measured line period in µs.
AVG_ABSC	22	word	Average apparent current in ADC units.
AVG_PHDC	24	word	Average phase-detected current in ADC units.
AVG_90DC	26	word	Average quadrature current in ADC units.
BANKS_ON	28	word	Total connected bank size in ADC units.

A.15.3. Bit I/O Progress Record

The bit I/O progress record fields are summarized in the following table:

Controller Bit I/O Progress Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
BINH_FLGS	0	byte	Current bit input 8-11 logical state flags
BINL_FLGS	1	byte	Current bit input 0-7 logical state flags
BOPH_FLGS	2	byte	Current bit output 8-11 logical state flags
BOPL_FLGS	3	byte	Current bit output 0-7 logical state flags
NEXT_BOPH	4	byte	Scheduled bit output 8-11 logical state flags
NEXT_BOPL	5	byte	Scheduled bit output 0-7 logical state flags
DISCHRGH_FLGS	6	byte	Current bank 8-11 active discharge flags
DISCHRGL_FLGS	7	byte	Current bank 0-7 active discharge flags

A.15.4. Error Data Progress Record

The error data progress record fields are summarized in the following table:

Controller Error Data Progress Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
ERFLGS	0	byte	Current error flags. b0: `Er.Sav`, b2: `nEt.Er`, b3: `Er.Prc`, b4: `Er.Com`, b5: `Er.Cmd`, b6: `Er.Src`, b7: `Er.Out`.
ERR_ADRS	1	word	`Er.Prc` source address.
ERRS_ATIDLE	3	byte	Last error flags
ERR_STATUS	4	byte	Last error status value
ERR_YEAR	5	integer	Last error system year
ERR_MONTH	7	byte	Last error system month
ERR_DATE	8	byte	Last error system day
ERR_HRS	9	byte	Last error system hour
ERR_MINS	10	byte	Last error system minutes
ERR_SECS	11	byte	Last error system seconds

A.15.5. Hardware Progress Record

The hardware readings progress record fields are summarized in the following table:

Controller Hardware Readings Progress Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
BIN_MSB_FLGS	0	byte	Bit input 8-11 states
BIN_LSB_FLGS	1	byte	Bit input 0-7 states
SW_INPS	2	byte	Panel switch states. b0: StArt/Stop, b1: Cntrl, b2: decr, b3: Incr.
ABS_CMEAS	3	word	Apparent ADC channel count
PHD_CMEAS	5	word	Phase-detected ADC channel count

A.15.6. Bank Size Progress Record

The bank size progress record fields are summarized in the following table:

Controller Bank Size Progress Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
BANK_INX_0	0	byte	Index to largest bank
BANK_INX_1	1	byte	Index to next largest bank
BANK_INX_2	2	byte	Index to next largest bank
BANK_INX_3	3	byte	Index to next largest bank
BANK_INX_4	4	byte	Index to next largest bank
BANK_INX_5	5	byte	Index to next largest bank
BANK_INX_6	6	byte	Index to next largest bank
BANK_INX_7	7	byte	Index to next largest bank
BANK_INX_8	8	byte	Index to next largest bank
BANK_INX_9	9	byte	Index to next largest bank
BANK_INX_10	10	byte	Index to next largest bank
BANK_INX_11	11	byte	Index to next largest bank

A.15.7. ADC Data Progress Record

The ADC data progress record fields are summarized in the following table:

Controller ADC Data Progress Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
ABS_CMEAS	0	word	Current apparent ADC channel count
PHD_CMEAS	2	word	Current phase-detected ADC channel count
AVG_ABSC	4	word	Average apparent current in ADC units.
AVG_PHDC	6	word	Average phase-detected current in ADC units.
AVG_90DC	8	word	Average quadrature current in ADC units.
AVG_ABS_OFS	10	word	Average apparent offset in ADC units.
AVG_PHD_OFS	12	word	Average phase-detected offset in ADC units.
ACCUM_ABS	14	long	Accumulated apparent sum in ADC units
ACCUM_PHD	18	long	Accumulated phase-detected sum in ADC units
AVG_SAMPL	22	word	No of accumulated ADC samples
AVG_TIME	24	word	Averaging/sampling time downcount in ticks.

A.15.8. Timestamp Progress Record

The timestamp progress record fields are as follows:

Controller Timestamp Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
YEAR	0	integer	Timestamp year
MONTH	2	byte	Timestamp month
DATE	3	byte	Timestamp day
HRS	4	byte	Timestamp hour
MINS	5	byte	Timestamp minutes
SECS	6	byte	Timestamp seconds

A.15.9. Bank Discharge Progress Record

The bank discharge progress record fields are summarized in the following table:

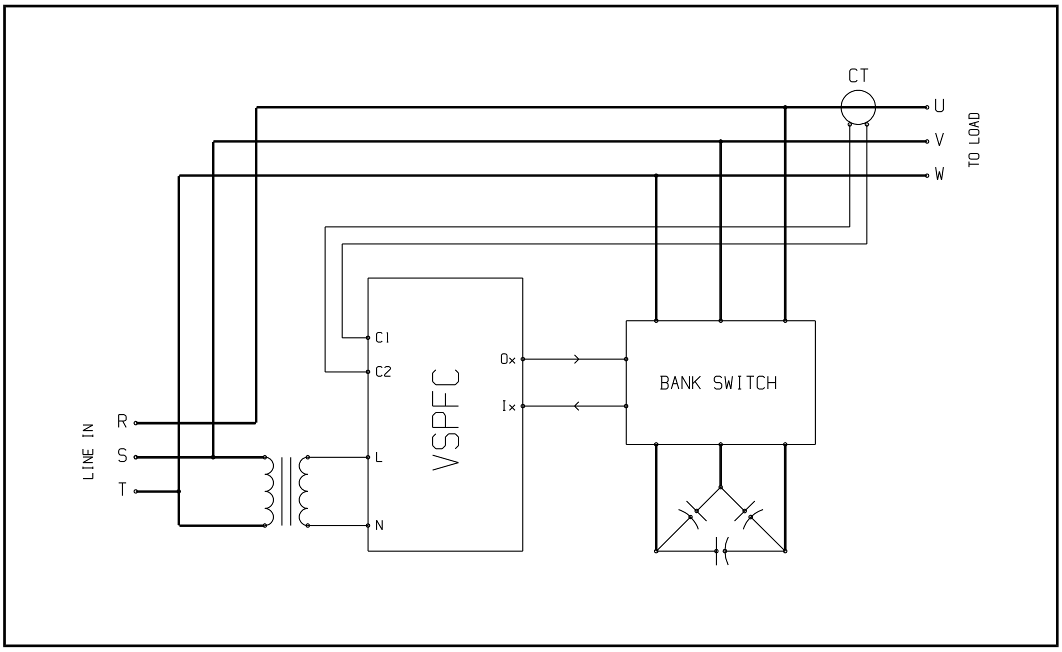
Controller Bank Size Progress Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
BANK_DIS_0	0	word	Bank 0 discharge tick downcount
BANK_DIS_1	2	word	Bank 1 discharge tick downcount
BANK_DIS_2	4	word	Bank 2 discharge tick downcount
BANK_DIS_3	6	word	Bank 3 discharge tick downcount
BANK_DIS_4	8	word	Bank 4 discharge tick downcount
BANK_DIS_5	10	word	Bank 5 discharge tick downcount
BANK_DIS_6	12	word	Bank 6 discharge tick downcount
BANK_DIS_7	14	word	Bank 7 discharge tick downcount
BANK_DIS_8	16	word	Bank 8 discharge tick downcount
BANK_DIS_9	18	word	Bank 9 discharge tick downcount
BANK_DIS_10	20	word	Bank 10 discharge tick downcount
BANK_DIS_11	22	word	Bank 11 discharge tick downcount

A.15.10. Controller Identity Record

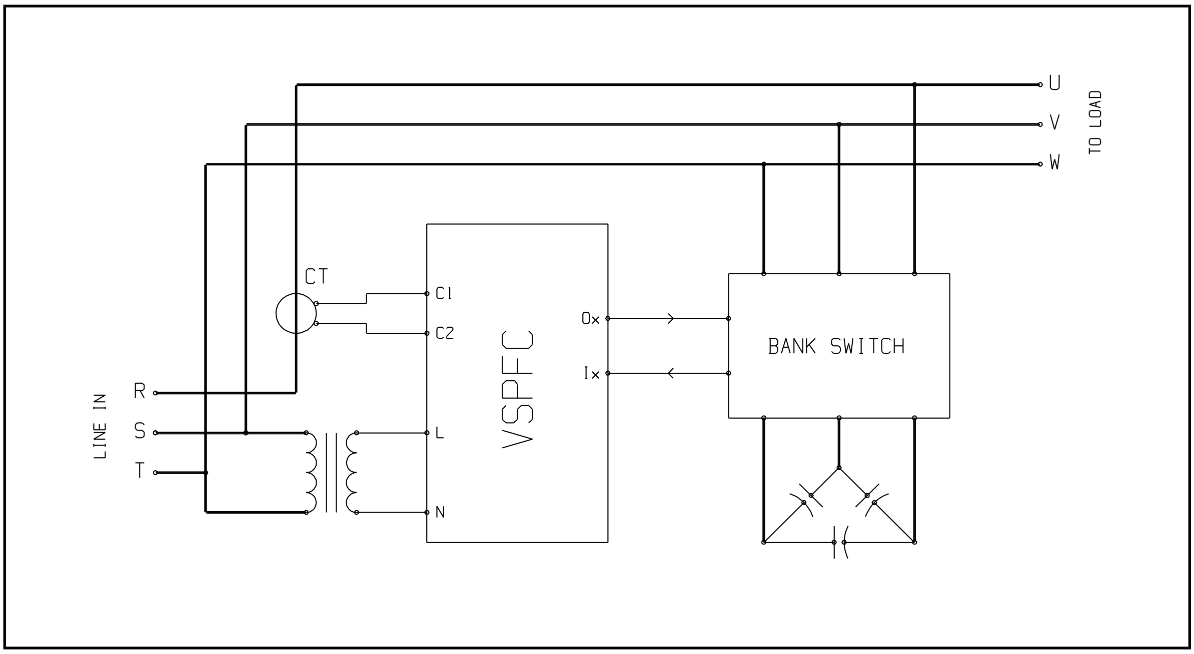
The Controller identity record fields are given below:

Controller Identity Record Fields			
Field	**Offset, Bytes**	**Type**	**Description**
GENUS	0	byte	Controller genre (=7)
TYPE	1	byte	Controller platform type (=2)
VERSION	2	byte	Software version (upper nibble, =0) and revision (lower nibble, =0)
PRC_CLOCK	3	byte	Processor clock in MHz, =12
TICKSPERSEC	4	byte	Controller ticks per second, =20
CNF_SIZE	5	word	Configuration record size, =84
PRG_SIZE	7	word	Full progress record size, =30
ACC_SIZE	9	word	Accumulated totals record size, =0 (none available)
RPRT_SZE	11	word	Generated report size, =0 (none available)
DSPL_INDX	13	word	Display index (`OPrtn` » `diSPL`) address
CNF_DOSE	15	word	Maximum configuration message length, =55
XOR_COMS	17	byte	XOR checksum capability, =5.
XTRA_FLVR	18	byte	Additional identity record bytes, =8.
CAL_SCUR_FCTR	19	long word	Factory calibrated ADC ampere factor (`SEtuP` » `Adc` » `A.Fctr`). Ampere factor = CAL_SCUR_FCTR/65536.
CAL_ABS_OFST	23	word	Factory calibrated apparent channel ADC offset (`SEtuP` » `Adc` » `Ab.oFS`).
CAL_PHS_OFST	25	word	Factory calibrated phase-detected channel ADC offset (`SEtuP` » `Adc` » `Ph.oFS`).

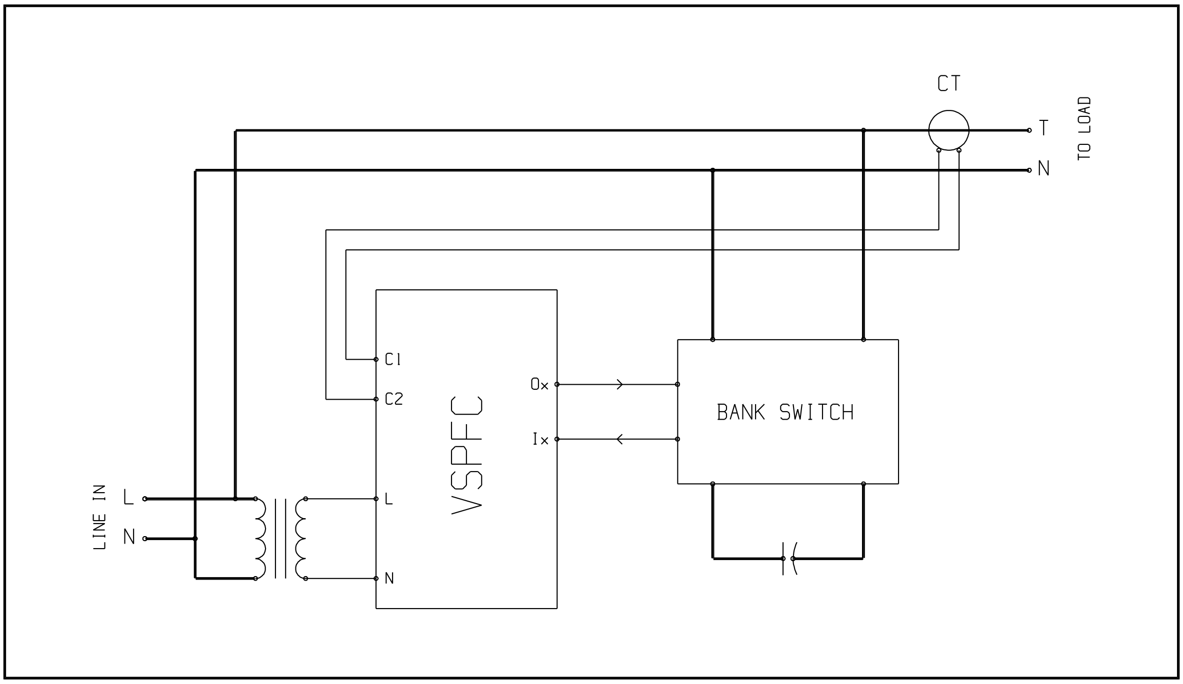
Appendix B. Connection Schematics



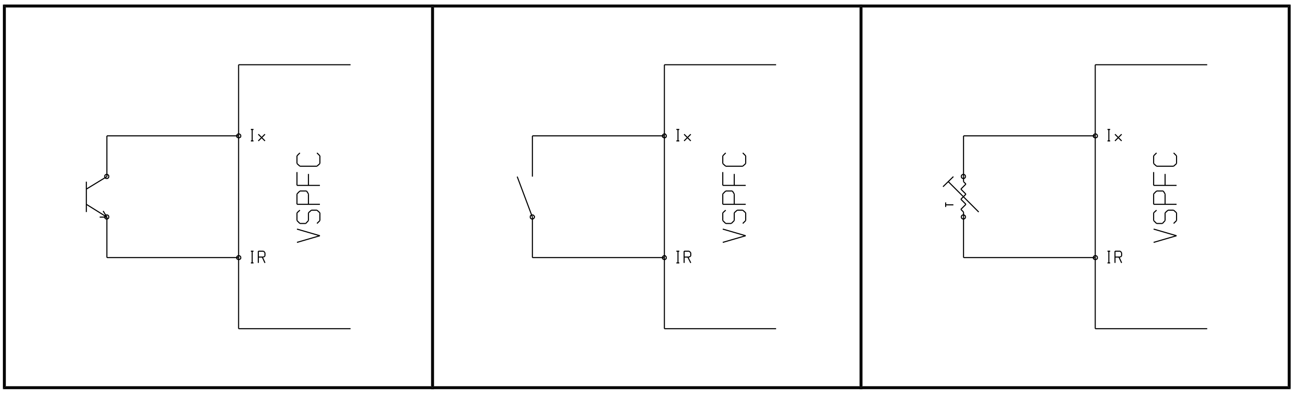
Three-phase VSPFC system operating in compensation mode. The current transformer (CT) detects the load current only at the U phase. The VSPFC supply is taken from the S and T phases and, as shown, a transformer is required when the line voltage is other than 220-240 VAC or to provide an isolated control supply line. The capacitor bank switches can interface bidirectionally with the VSPFC.



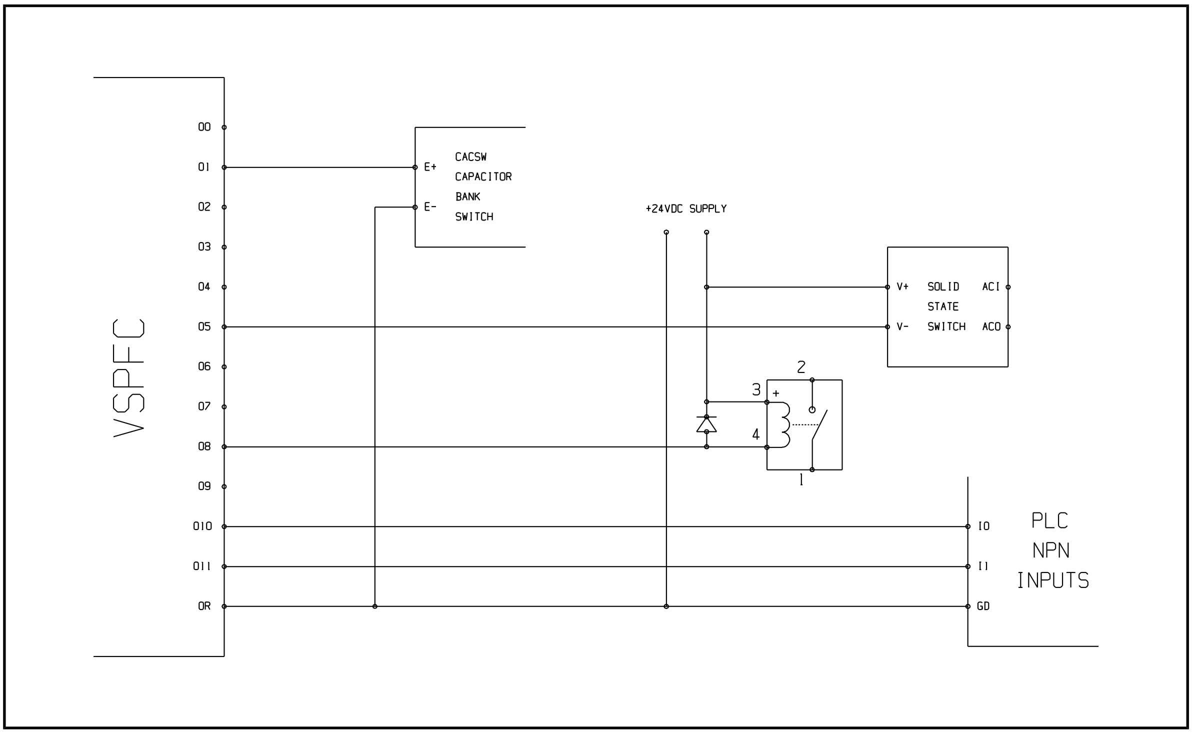
Three-phase VSPFC system operating in regulation mode. The current transformer (CT) detects the load current plus any compensating capacitor bank current at the R phase. The VSPFC supply is taken from the S and T phases and, as shown, the transformer is required when the line voltage is other than 220-240 VAC or to provide an isolated control supply line. The capacitor bank switches can interface bidirectionally with the VSPFC.



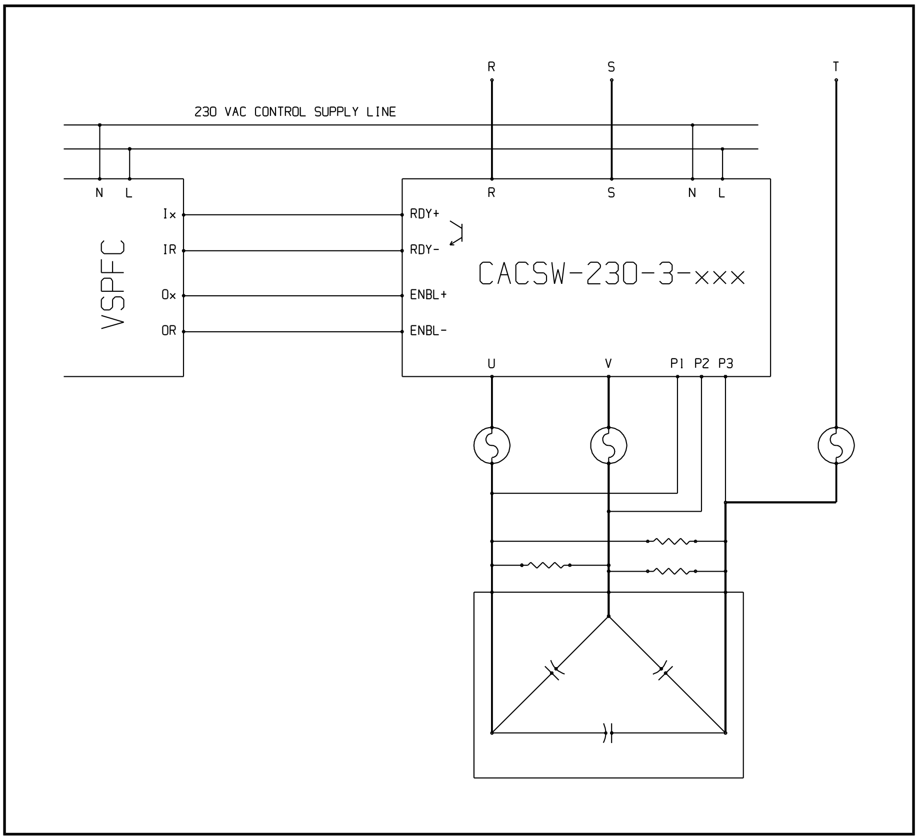
Single-phase VSPFC system operating in compensation mode. (Regulation mode is not possible in single-phase systems). The current transformer (CT) detects the load current only at phase T. The transformer at the VSPFC supply is required when the phase voltage is other than 220-240 VAC or to provide an isolated control supply line. The capacitor bank switches can interface bidirectionally with the VSPFC.



VSPFC enable bit inputs driven by an open collector, NPN, current sink source (left), switch or relay contacts (middle) and PTC thermistor (right).



VSPFC bit outputs driving various loads: a CACSW bank switch, a solid state realay (SSR), a small relay and PLC inputs.



Direct VSPFC interface to a CACSW capacitor bank switch. The CACSW is driven by the VSPFC, detects the capacitor fuses state and reports it via its "Ready" output. In this example they are powered by a 230 VAC control supply which is separate from the three-phase power lines.